

1 **ABSTRACT OF THE DISCLOSURE**

2 A method for testing memories has steps of providing seamless data to
3 data input/output pins and providing seamless control commands to each
4 bank at each clock cycle, when the memories receive the seamless data and
5 control commands, and the data input/output pins of memories receive
6 heavy loads status. For SDRAM and DDR-DRAM, control commands and
7 data are seamlessly inputted/outputted at each clock cycle. For RDRAM,
8 control commands are inputted at each “command packet”, whereby data
9 are inputted/outputted at each “data packet” and memories are in the heavy
10 loading status. By providing heavy loading to control pins and data
11 input/output pins of memories, it is easy to detect weakened memories.